

**AMENDMENTS TO THE CLAIMS**

## Claim 1-49 (Cancelled)

50. (Previously Presented) A method for testing a television, comprising:  
selecting a data pattern from a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern of the set of at least one pre-programmed data pattern includes a plurality of portions;  
creating the selected data pattern, wherein creating the selected data pattern includes:  
for each of the plurality of portions of the selected data pattern that is pre-programmed for algorithmic pattern generation, performing a pre-programmed algorithm to create the portion; and  
for each of the plurality of portions of the data patterns that is stored based on the pre-programming of the selected data pattern, retrieving the portion.
51. (Previously Presented) The method of Claim 50, further comprising:  
determining and storing at least one checksum for each of the at least one pre-programmed data pattern;  
generating at least one BIST checksum from the created data pattern; and  
comparing the at least one BIST checksum with the at least one stored checksum for the created data pattern.
52. (Previously Presented) The method of Claim 50, wherein the algorithmic pattern generation is accomplished, in part, by a state machine.
53. (Previously Presented) The method of Claim 52, further comprising:  
determining if a different data pattern is selected; and  
if a different data pattern is selected:  
asserting a pattern change signal; and







72. (Previously Presented) The method of Claim 70, wherein configuring the memory component is further accomplished such that the tables further include a colour table, a PLL pathological table, and an equalizer pathological table for algorithmic pattern generation of active video lines.

73. (Previously Presented) The method of Claim 72, wherein configuring the memory component further includes configuring logic for the equalizer pathological table for selecting between two elements based on a line number and further based on which of the at least one data pattern is selected.

74. (Previously Presented) A method for testing a television, comprising:  
generating a computer-readable algorithm that is configured to provide at least one portion of a plurality of portions of a data pattern through algorithmic pattern generation; and  
storing at least one other portion of the plurality of portions in a look-up table.

75. (Currently amended) The method of Claim 74, further comprising:  
generating at least one other computer-readable algorithm that is configured to provide at least one other portion of a plurality of portions of another data pattern through algorithmic pattern generation such that the computer-readable algorithm and the other computer-readable algorithm comprise a plurality of computer-readable algorithms that are stored in a computer-readable medium, and such that the computer-readable medium is configured to regenerate a plurality of data patterns including the data pattern and the other data pattern;  
storing at least one other portion of the other data pattern in the look-up table;  
selecting a data pattern from the plurality of data patterns;  
creating the selected data pattern based on at least one of the computer-readable algorithms and further based on the other portion of the plurality of portions of the selected data pattern.



82. (Previously Presented) The method of Claim 81, wherein configuring the memory component further includes configuring logic for the equalizer pathological table for selecting between two elements based on a line number and further based on which of the plurality of data patterns is selected.

83. (Currently amended) A test circuit for a television, comprising:

a pattern selection register that is arranged to store and provide a pattern select value indicating a selected data pattern of a set of at least one pre-programmed data pattern, wherein each pre-programmed data pattern in the set of at least one pre-programmed data pattern includes a plurality of portions;

a look-up table component that stores a portion in the plurality of portions of each of the pre-programmed data patterns in the set of at least one pre-programmed data pattern; and

a state machine that is configured to enable the selected data pattern to be generated based on the pattern selection value, wherein state machine is configured to enable the selected data pattern to be generated by:

controlling a retrieval of the portion of the selected data pattern from the look-up table component; and

based on the pre-programming, controlling a sequencing for algorithmic pattern generation of another portion of the selected data pattern.

84. (Previously Presented) The test circuit of Claim 83, wherein the state machine is configured to control both the retrieval of the portion and the other portion by providing a plurality of clear and increment signals.

85. (Previously Presented) The test circuit of Claim 84, wherein the look-up table component is configured to generate a table output signal based on the clear and increments signals, and further based on the pattern select value.

86. (Previously Presented) The test circuit of Claim 85, further comprising an output register that is configured to generate the selected data pattern from the data output signal.

87. (Previously Presented) The test circuit of Claim 85, wherein the look-up table component includes a plurality of look-up tables including a header table.

88. (Previously Presented) The test circuit of Claim 87, wherein at least one of the plurality of look-up tables stores part of a repeating data sequence, and further stores a value indicating a number of times that the part of the repeating data sequence is to be repeated.

89. (Previously Presented) The test circuit of Claim 87, wherein the header table includes data for algorithmic pattern generation of vertical blanking lines.

90. (Previously Presented) The test circuit of Claim 87, further comprising a line index table component that stores values indicating when to the state machine is to control switching to and from the vertical blanking lines to active video lines.

91. (Previously Presented) The test circuit of Claim 87, wherein the plurality of look-up tables further include a colour table, a PLL pathological table, and an equalizer pathological table.

92. (Previously Presented) The test circuit of Claim 91, further comprising a plurality of logic gates for selecting between two elements for reading from an equalizer pathological table such that the selection between the two elements is based on a line number and further based on the pattern select value.

93. (Previously Presented) The test circuit of Claim 83, further comprising:  
a built-in self test circuit that is arranged to perform actions, including:  
during a configuration, determining and storing at least one checksum for each of the plurality of component video data patterns;



determining at least one checksum for the regenerated selected data pattern; and  
comparing the at least one checksum for the regenerated selected data pattern with  
the at least one stored checksum for the selected data pattern; and  
a BIST result output pin that is configured to provide a BIST result signal that indicates a  
result of the checksum comparison.

94. (Previously Presented) A test circuit for a television, comprising:

a look-up table component that is configurable to store a portion of each of a plurality of  
data patterns;

a state machine that is configurable to provide, if one of the plurality of data patterns is  
selected, a sequencing for algorithmic pattern generation of another portion of the selected data  
pattern;

an output register that is configured to provide a regenerated selected data pattern based, in  
part, on the sequencing; and

a built-in self test circuit that is configured to perform actions, including:

during a configuration, determining and storing at least one checksum for each of the  
plurality of data patterns;

determining at least one checksum for the regenerated selected data pattern; and

comparing the at least one checksum for the regenerated selected data pattern with  
the at least one stored checksum for the selected data pattern.

95. (Previously Presented) A test circuit for a television, comprising:

a pattern selection register that is arranged to store and provide a pattern selection value  
indicating a selected data pattern of a plurality of component video data patterns, wherein each  
component video data pattern in the plurality of component video data patterns includes a plurality  
of portions;

a pattern generation state machine that is arranged to control a sequencing of a regeneration  
of the selected data pattern by providing a plurality of clear and increment signals;



divided into five sample segments; and wherein each of the five sample segments includes four 10-bit samples, and further includes a repeat value that indicates to the state machine how many times the four 10-bit samples are to be repeated.

97. (Currently amended) A method for testing a television, comprising:
- configuring a state machine with, for each of a plurality of component video data patterns, a sequencing for regenerating each of the component video data patterns;
  - configuring a header table to store:
    - a plurality of forty-bit data samples that each include a unique data word; and
    - a sequence of data that includes a portion of a repeating vertical blanking data sequence for vertical blanking lines, and further includes a repeat field that indicates a number of repetitions for the repeating vertical blanking sequence;
  - configuring a line index table to store values indicating a number of lines to transmit before switching to and from the vertical blanking lines to active video lines;
  - configuring a colour table, a PLL pathological table, and an equalizer pathological table for algorithmic pattern generation of portions of each of the plurality of component video data patterns for the active video lines;
  - determining and storing at least one checksum for each of the plurality of component video data patterns;
  - selecting one of the plurality of component video patterns;
  - providing a plurality of clear and increment signals based on the sequencing for regenerating the selected component video pattern;
  - employing the header table, the colour table, the PLL pathological table, the equalizer pathological table, and the line index table to regenerate the selected data pattern based, in part, on the plurality of clear and increment signals;
  - concurrently:
    - displaying a video picture based on the regenerated selected test pattern; and
    - providing the regenerated selected test pattern to a built-in self test circuit; and
  - employing the built-in self test circuit to:

generate at least one BIST checksum from the regenerated selected data pattern;  
compare the at least one BIST checksum with the at least one stored checksum for  
the selected data pattern; and  
provide a result of the comparison to a BIST result output pin.

98. (Currently amended) The method of Claim 97, wherein the plurality of component video ~~patterns signals~~ includes at least sixteen component video ~~signals patterns~~; regeneration of the selected data ~~pattern signal~~ is provided based on a relatively small number of data words including the plurality of forty bit data samples and the sequence of data; configuring the at least one look-up table is accomplished such that each look-up table of the at least one look-up table is divided into five sample segments; and wherein each of the five sample segments includes four 10-bit samples, and further includes a repeat value that indicates how many times the four 10-bit samples are to be repeated.

99. (New) The method of Claim 61, wherein  
pre-programming the at least one data pattern is accomplished according to the method of Claim 82.

100. (New) The method of Claim 61, further comprising:  
determining and storing at least one checksum for each data pattern of the set of at least one data pattern, wherein creating the selected test pattern includes regenerating the selected test pattern;  
concurrently:  
displaying a video picture based on the regenerated selected test pattern; and  
providing the regenerated selected test pattern to a built-in self test circuit; and  
employing the built-in self test circuit to:  
generate at least one BIST checksum from the regenerated selected data  
pattern;  
compare the at least one BIST checksum with the at least one stored  
checksum for the selected data pattern; and





when the data pattern is selected, starting the state machine and initiating sample, packet, and look-up signals; and

creating the selected data pattern from at least a look-up table component and a state machine by performing actions, including:

tracking a location in a data sequence of the selected test pattern and transitioning between states according to the pre-programming by providing a plurality of clear and increment signals from the state machine;

employing the look-up table component to regenerate the selected data pattern based, in part, on the plurality of clear and increment signals, wherein the look-up table component includes a plurality of look-up tables, and wherein plurality of look-up tables includes a header table, a colour table, a PLL pathological table, an equalizer pathological table, and a line index table;

filtering an output of at least one of the state machine and the plurality of look-up tables; and

dithering an output of at least one of the state machine and the plurality of look-up tables.

105. (New) The method of Claim 104, wherein  
pre-programming the at least one data pattern is accomplished according to the method of Claim 74.

106. (New) The method of Claim 104, wherein  
pre-programming the at least one data pattern is accomplished according to the method of Claim 82.

107. (New) The method of Claim 104, wherein  
pre-programming the at least one data pattern includes:









determining at least one checksum for the regenerated selected data pattern; and  
comparing the at least one checksum for the regenerated selected data pattern with  
the at least one stored checksum for the selected data pattern.

113. (New) The test circuit of Claim 92, further comprising:

a built-in self test circuit that is arranged to perform actions, including:

during a configuration, determining and storing at least one checksum for each of the  
plurality of component video data patterns;

determining at least one checksum for the regenerated selected data pattern; and  
comparing the at least one checksum for the regenerated selected data pattern with  
the at least one stored checksum for the selected data pattern; and

a BIST result output pin that is configured to provide a BIST result signal that indicates a  
result of the comparison, wherein the look-up table component is a memory component, and  
wherein the header table stores:

a plurality of forty-bit data samples that each include a unique data word; and  
a sequence of data that includes a portion of a repeating vertical blanking data  
sequence for the vertical blanking lines, and further includes a repeat field that indicates a  
number of repetitions for the repeating vertical blanking sequence.

114. (New) The test circuit of Claim 94, further comprising:

a pattern selection register that is arranged to store and provide a pattern select value  
indicating the selected data pattern, wherein each of the plurality of data patterns is pre-  
programmed, and wherein the state machine is further configured to control a retrieval of the  
portion of the selected data pattern from the look-up table component.

115. (New) The test circuit of Claim 94, further comprising:

a pattern selection register that is arranged to store and provide a pattern select value  
indicating the selected data pattern, wherein each of the plurality of data patterns is a component  
video data pattern;



118. (New) The method of Claim 98, wherein  
the method is accomplished by employing the test circuit of Claim 96, and wherein the state  
machine is the pattern generation state machine.